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Wave-digital filter circuits for single-chip 4-D light field depth-based enhancement

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Abstract
In four-dimensional (4-D) light field (LF) processing, 4-D linear shift-invariant filters having hyperplanar passbands are used for depth-based scene enhancement. In this paper, two low-sensitivity and low-complexity field programmable gate array (FPGA)-based digital hardware architectures for 4-D hyperplanar filters are proposed for on-chip real-time processing of LFs. Both 4-D filters are designed exploiting resonant properties of multi-dimensional passive prototype networks, and are realized as wave digital filters (WDFs). The two 4-D WDF realizations are implemented as raster-scanned processing architectures on a Xilinx Virtex 6 Sx35 FPGA with a real-time clock speed of up to 33 MHz. This corresponds to a real-time throughout of 16.8 LFs/s for an LF of size $11 \times 11 \times 128 \times 128$.

Keywords Light fields · Wave digital filters · Low sensitivity · Real-time depth filtering

1 Introduction

Light field (LF) based computational imaging captures the angular variation of light emanating from a scene as a function of spatial position. An LF image takes the form of a four-dimensional (4-D) data hybercube (a tensor) that embeds both textural and geometric information of a scene such that linear processing operations on a 4-D LF furnishes a range of imaging capabilities, including post-capture refocusing, occlusion removal, visual odometry and depth-based image enhancement (Dansereau and Bruton 2007, 2003, 2004; Levin et al. 2009; Dansereau et al. 2015; McCloskey 2014; Wang et al. 2015; Premaratne et al. 2018; Liyanage et al. 2019). Furthermore, LFs can be employed for depth estimation (Wanner and Goldluecke 2012; Tao et al. 2013; Wang et al. 2015, 2016; Chang et al. 2014; Chen et al. 2018; Domínguez Conde et al. 2019) of scenes and wavefront sensing (Rodríguez-Ramos et al. 2010, 2012; Chen et al. 2020). Moreover, LFs find multiple applications in artificial intelligence and computer vision systems aimed at mobile robotics in particular (Dong et al. 2013; Tsai et al. 2017; Bajpayee et al. 2018). Due to the large volume of input samples typically encountered in LFs, custom computing digital hardware architectures are of com-

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mon interest to realize a multitude of signal processing algorithms in real-time (Liyanage et al. 2019; Wijenayake et al. 2019; Madanayake et al. 2015; Wimalagunarathne et al. 2013; Hahne and Aggoun 2014a). Moreover, digital hardware realizations having low sensitivity properties to fixed point quantization effects are of interest to minimally compromise the output quality when achieving low complexity and real-time processing.

From classical circuit theory, doubly-terminated passive networks show the lowest sensitivity to changes in the reactive elements (Bruton 1980). This low-sensitivity property extends to multi-dimensional (MD) doubly-terminated passive networks. The application of the bilinear transform (BLT) to such MD passive networks results in corresponding MD infinite impulse response (IIR) digital filters (Zhang and Bruton 1994), which are guaranteed to be practical bounded input bounded output (P-BIBO) stable (Agathoklis and Bruton 1983), while showing low sensitivity to errors in filter coefficients. Doubly-terminated passive networks can be designed that, for frequencies of minimum loss (i.e., passband), the source delivers maximum available power to the load. The derivative of the loss with respect to reactive components in the network, such as inductors and capacitors, is zero. The "Orchard's Argument" states that the frequency points where minimum loss occurs are few, the frequencies in their neighborhood have low valued derivatives, and therefore, by definition of sensitivity, have corresponding low sensitivity if not zero sensitivity (Bruton 1980; Orchard 1966; Temes and Orchard 1973).

Wave-digital filters (WDFs) (Fettweis 1986) are a type of digital filters that uses direct digitization of the forward and backward scattering wave components using the BLT, such that there is structural similarity between the original analog prototype and the bilinear transformed digital filter. Therefore, WDFs can be shown to have the lowest possible sensitivity to filter coefficient quantization compared to other structures such as direct-form and integral-form digital filters, which are also designed using the BLT (Fettweis 1986). The WDFs also posses superior round-off noise performance compared to alternative digital filter structures. In this paper, we exploit WDFs to propose computational architectures for 4-D LF digital filters that are based on doubly-terminated passive 4-D prototype networks (Zhang and Bruton 1994). To the best of our knowledge, the proposed design is the first 4-D WDF architecture used in the context of LF processing applications. In particular, our contributions in this paper are: (i) extending the previously reported WDF architectures in 2-D and 3-D (Rajapaksha et al. 2015; Li et al. 2009; Schauland et al. 2008) to the 4-D case and demonstrate their use as depth selective filters in 4-D LFs; (ii) provide closed-form design equations to WDF coefficients allowing fast tuning of filter passbands to a required depth; (iii) present a raster-scanned custom computing digital hardware architecture along with prototype field programmable gate array (FPGA) implementation and validation.

2 Related work

2.1 4-D linear filters employed for LF processing

Selective filtering of objects in 4-D LFs was first demonstrated in (Isaksen et al. 2000). Here, it was shown that objects occupied in a narrow-depth range can be significantly attenuated using a 4-D finite impulse response (FIR) filter. Similar results, using a low-complexity 4-D IIR filter was presented in (Dansereau and Bruton 2003). This 4-D filter was designed by cascading two 4-D IIR filters having hyperplanar passbands which were obtained exploiting the resonance of a 4-D passive resistor-inductor network. A 4-D IIR depth filter with a

hyperfan passband that can be used to selectively filter objects occupied in a wide-depth range was presented in (Dansereau and Bruton 2007). This 4-D filter was designed using a filter bank approach with 4-D IIR hyperplanar filters reported in (Dansereau and Bruton 2003). Recently, a low-complexity 4-D IIR filter with multiple hyperplanar passbands and hyperplanar stopbands was proposed in (Liyanage et al. 2018). This filter can be employed to simultaneously enhance and attenuate objects occupied in multiple narrow-depth ranges.

A 4-D FIR filter was proposed in (Ng et al. 2005) for LF refocusing, where objects occupied in a selected narrow-depth range is enhanced while blurring the objects in other depths. Similar results were reported in (Ng 2005; Veeraraghavan et al. 2007) and (Lumsdaine and Georgiev 2009). A 4-D FIR filter having a hyperfan passband was proposed in (Dansereau et al. 2015) to refocus a wide-depth range (called volumetric refocusing) of a LF. A similar filter is employed for LF denoising in (Dansereau et al. 2013) and, with reduced computational complexity, in (Premaratne et al. 2020), where all the objects in a LF are enhanced while attenuating noise. Recently, low-complexity 4-D hyperfan FIR filters were proposed in (Premaratne et al. 2018) and in (Jayaweera et al. 2020) for volumetric refocusing a single region and multiple regions, respectively. Compared to the 4-D FIR filter proposed in (Dansereau et al. 2015), these filters provide significant reduction in computational complexity. Furthermore, spatial modulation with a sparse window function was applied in (Liyanage et al. 2019) to considerably reduce the computational complexity of both 4-D FIR and IIR depth filters.

2.2 Hardware architectures of 4-D linear filters

Hardware architectures for 4-D IIR hyperplanar depth filters were first presented in (Madanayake et al. 2011a) and (Wimalagunarathne et al. 2012), where a scanned-array and a semi-systolic array architectures, respectively, were implemented in FPGAs for real-time depth filtering. Furthermore, low-complexity differential-form and integral-form hardware architectures were proposed in (Madanayake et al. 2015) and (Wimalagunarathne et al. 2013), respectively, extending the work presented in (Madanayake et al. 2011a) and (Wimalagunarathne et al. 2012). A low-complexity embedded design of a 4-D FIR filter was proposed in (Hahne and Aggoun 2014b) for real-time refocusing using linear interpolation and averaging. In (Hahne et al. 2018), a similar low-complexity 4-D FIR filter was implemented in FPGAs. Recently, FPGA implementations of semi-systolic hardware architectures for 4-D IIR multi-depth filters and five-dimensional (5-D) IIR depth-velocity filters (employed for processing of 5-D LF videos) (Edussooriya et al. 2015b, a) were presented in (Liyanage et al. 2019) and (Wijenayake et al. 2019), respectively, achieving real-time operation.

2.3 Multidimensional WDFs and VLSI implementations

WDFs—invented by Alfred Fettweis—has received much attention in the literature for one-dimensional and MD signal processing(Fettweis 1986). The reader is referred to (Fettweis 1986) for original work on WDFs, and (Fettweis and Meerkotter 1975; Meerkötter 2018) for previous theoretical work on the extension of WDF concepts to MD linear filters. Despite digital very large scale integration (VLSI) implementations of two-dimensional (2-D) WDFs on FPGAs reported for beamforming (Rajapaksha et al. 2015) and three-dimensional (3-D) WDFs on FPGAs reported for imaging applications (Li et al. 2009; Schauland et al. 2008), VLSI implementations of MD WDFs is, however, relatively unknown. Although several 4-D/5-D digital VLSI architectures based on direct-, differential and integral-form signal flow graphs (SFGs) have been reported (Madanayake et al. 2015; Wimalagunarathne et al. 2013;

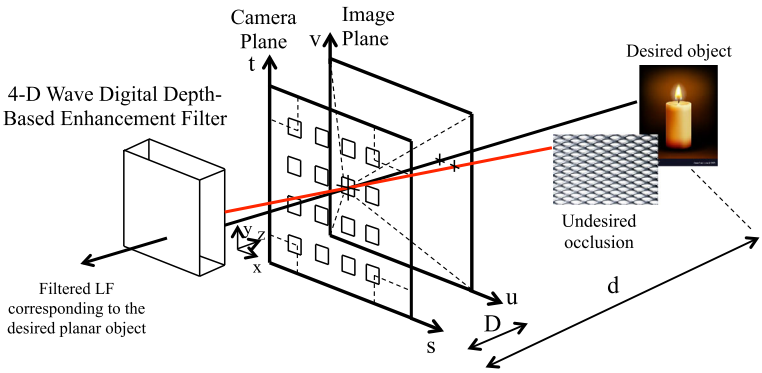

Fig. 1 Overview of the depth-based enhancement of LFs with the proposed 4-D WDF. The figure shows a pictorial representation of a scene on the right, containing a desired object (i.e., the candle) and an undesired object (i.e., the mesh) with the corresponding light rays represented by the black and red lines, respectively. The two-plane parameterization represents the input light field captured by a light field acquisition hardware, which is then processed by the proposed WDF-based depth filter, denoted by the box on the left. After such filtering the light rays emanating from the desired object are retained and while the light rays emanating from the undesired object are attenuated, thereby providing a depth-based enhancement of the scene (Color figure online)

Wijenayake et al. 2019), to the best of our knowledge, corresponding VLSI implementations of WDFs using FPGAs have not been reported.

3 Wave digital 4-D IIR depth filters

3.1 Depth-based enhancement of 4-D LFs

A pictorial overview of depth-based enhancement of LFs using the proposed 4-D WDFs is shown in Fig. 1, where a desired passband object at a given depth is selectively enhanced while attenuating and blurring undesired objects for occlusion removal and refocusing, respectively. As pictorially represented in Fig. 1, a scene containing a desired object and an undesired object (such as a partial occlusion) is captured through a LF acquisition hardware, which is represented by the two-plane parametrization (Levoy and Hanrahan 1996), containing two parallel planes known as the camera plane and the image plane, which (approximately) model the light rays emanating from the scene taking into account four spatial coordinates, thus allowing for a convenient 4-D signal processing model. Thus captured scene, modeled by a 4-D spatial discrete-domain signal is then processed by the proposed 4-D WDF to selectively attenuate spectral components corresponding to the undesired object. Here, 4-D WDFs are designed to have planar passbands in the 4-D frequency domain. This planar passband encompasses the region of support (ROS) of the spectrum of the desired object in the 4-D LF, which is defined for a Lambertian planar object as (Dansereau and Bruton 2003; Chai et al. 2000)

$$\mathscr{R}_p = \mathscr{H}_{su} \cap \mathscr{H}_{tv}, \tag{1}$$

where

$$\mathscr{H}_{su} = \left\{ \boldsymbol{\omega} \in \mathscr{N} \;\middle|\; \omega_s - \left(\frac{D \Delta s}{z_0 \Delta u} \right) \omega_u = 0 \right\} \tag{2a}$$

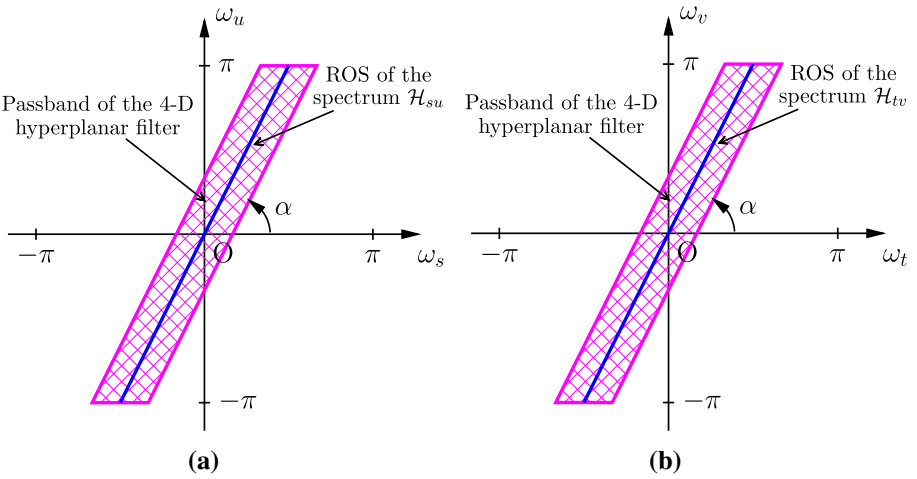

Fig. 2 **a** The ROS of the spectrum $\mathscr{H}_{su}$ of the desired object to be enhanced (solid) and the passband of the 4-D hyperplanar filter (cross-hatched) in the $\omega_s\omega_u$ plane; **b** the ROS of the spectrum $\mathscr{H}_{tv}$ of the desired object to be enhanced (solid) and the passband of the 4-D hyperplanar filter (cross-hatched) in the $\omega_t\omega_v$ plane. When $\Delta s = \Delta t$ and $\Delta u = \Delta v$, both $\mathscr{H}_{su}$ and $\mathscr{H}_{tv}$ have the same orientation, which depends on the depth z_0 of the desired object

$$\mathscr{H}_{tv} = \left\{ \boldsymbol{\omega} \in \mathscr{N} \;\middle|\; \omega_t - \left(\frac{D\Delta t}{z_0 \Delta v} \right) \omega_v = 0 \right\}. \tag{2b}$$

Here, $\boldsymbol{\omega} = (\omega_s, \omega_t, \omega_u, \omega_v) \in \mathbb{R}^4$ is the 4-D frequency domain associated with the 4-D spatial domain corresponding to sampled LFs, $\mathscr{N}$ is the 4-D Nyquist hypercube, z_0 is the depth of the Lambertian planar object, D is the distance between the camera plane and the image plane of the two-plane parametrization (Levoy and Hanrahan 1996) (see Fig. 1), and $\Delta i, i = s, t, u, v$, is the sampling interval along the corresponding dimension. Note that the planar spectral ROS $\mathscr{R}_p$ is defined by the intersection of *two 4-D hyperplanes* $\mathscr{H}_{su}$ and $\mathscr{H}_{tv}$. Furthermore, D and Δi, $i = s, t, u, v$ are constants for a given LF, and the orientation of the spectral ROS $\mathscr{R}_p$ depends only on the depth z_0 of the Lambertian object (Dansereau and Bruton 2003; Chai et al. 2000). Based on this spectral property, 4-D depth-based enhancement of planar objects in an LF can be achieved by a suitable 4-D discrete-domain filter having a frequency planar passband. Such 4-D planar filters are designed as a cascade of two 4-D hyperplanar filters (Dansereau and Bruton 2003). The 4-D hyperplanes $\mathscr{H}_{su}$ and $\mathscr{H}_{tv}$ with the passband of 4-D hyperplanar filters are shown in Fig. 2a, b, respectively. With typical sampling employed in LF capturing, where $\Delta s = \Delta t$ and $\Delta u = \Delta v$, the angle α between a hyperplanar passband and ω_s or ω_t axis is given by

$$\alpha = \tan^{-1}\left(\frac{z_0 \Delta}{D} \right), \tag{3}$$

where $\Delta = \frac{\Delta u}{\Delta s} = \frac{\Delta v}{\Delta t}$. Note that α varies from 0° to 90° when depth z_0 varies from 0 to ∞.

An example of refocusing using 4-D IIR planar filters (Dansereau and Bruton 2003) is shown in Fig. 3 for the LF "Flowers" in the EPFL LF dataset (Rerabek and Ebrahimi 2016). It can be clearly observed that the 4-D IIR planar filter designed to enhance the foreground and the background, respectively, successfully performs the depth-based enhancement.

Fig. 3 Refocusing of the "Flowers" LF using 4-D IIR planar filters **a** focused to the foreground, **b** focused to the background. Note that only a single sub-aperture image of the LF is shown (Color figure online)

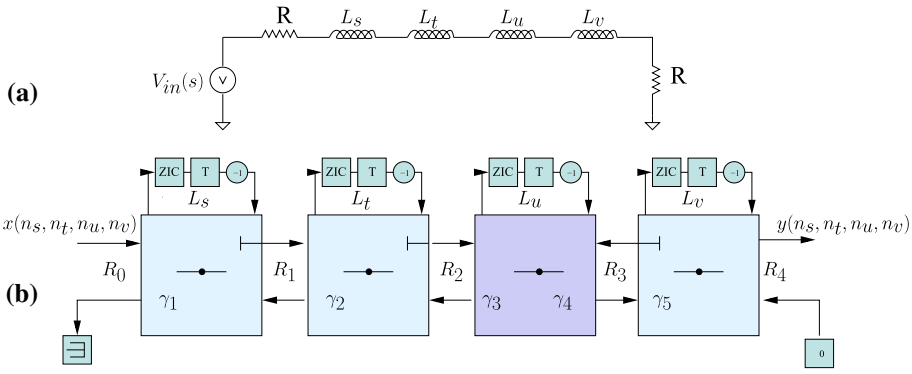

Fig. 4 **a** Passive prototype for the 4-D non-separable hyperplanar filter building block; **b** WDF realization

3.2 Design of wave-digital 4-D IIR depth filters

In this work, the proposed 4-D IIR depth enhancement WDFs are synthesized using a doubly (resistively) terminated 4-D IIR hyperplanar filters. The 4-D first-order IIR hyperplanar filter, shown in Fig. 4a, consists of a 4-D series inductance, load resistance R and source resistance R, such that, the prototype 4-D continuous domain transfer-function is given by

$$H_{hp}(\mathbf{s}) = \frac{R}{2R + L_s s_s + L_t s_t + L_u s_u + L_v s_v}, \tag{4}$$

where $\mathbf{s} = (s_s, s_t, s_u, s_v) \in \mathbb{C}^4$, and $L_{s,t,u,v} \geq 0$ for passivity. For brevity, let us abbreviate $L_s s_s + L_t s_t + L_u s_u + L_v s_v$ as $\sum L_k s_k$, $k = \{s, t, u, v\}$. The digital realization is achieved for the direct-form SFG by directly mapping the Laplace variables to their z-domain counterpart

using the normalized 4-D BLT $s_k = \frac{z_k - 1}{z_k + 1}$, $z_k \in \mathbb{C}$. Integro-differential forms are also available using derivatives of the above method (Zhang and Bruton 1994; Wimalagunarathne et al. 2013). In this paper, instead of digitization of the transfer function of the prototype network defined in voltage/current domains, we employ forward and reverse wave models that lead to the corresponding wave-digital filter realization. The WDF realization is structurally similar to the doubly-terminated passive prototype network, which enables the low-sensitivity properties to transfer to digital filter coefficients that define each first-order difference equation for passive components in the network (Fettweis 1986).

The first wave digital 4-D filter having a planar passband is designed by cascading two 4-D *non-separable* IIR hyperplanar filters defined in (4) (Dansereau and Bruton 2003) as

$$H_{ns}(\mathbf{s}) = \frac{R}{2R + \sum L_k s_k} \cdot \frac{R}{2R + \sum L_k s_k}. \tag{5}$$

The corresponding 4-D IIR digital hyperplanar filter building block can be obtained with the 4-D BLT as

$$T_{ns}(\mathbf{z}) = \frac{R}{2R + \sum_{k\in\{s,t,u,v\}} L_k \frac{z_k - 1}{z_k + 1}} \cdot \frac{R}{2R + \sum_{k\in\{s,t,u,v\}} L_k \frac{z_k - 1}{z_k + 1}}, \tag{6}$$

where $\mathbf{z} = (z_s, z_t, z_u, z_v) \in \mathbb{C}^4$. The depth filtering on a 4-D light-field is achieved by cascading two of these building blocks such that the region of intersection falls on the region of support (ROS) of the desired signal in the 4-D frequency domain.

In (Dansereau and Bruton 2007), it has been shown that 4-D non-separable IIR hyperplanar filters can be simplified to 2-D IIR beam filters if the orientation of the hyperplanar passband depend only on two dimensions and independent of other two dimensions. This simplification leads to approximately 75% reduction in number of additions required to process a sample, and the software implementation presented in (Dansereau and Bruton 2007) achieved 1.7 times reduction in the processing time compared to a depth filter based on 4-D non-separable IIR hyperplanar filters. Using this property, the second wave digital 4-D filter, shown in Fig. 5a, is designed as a 4-D *partially-separable* IIR planar filter $H_{ps}(\mathbf{s})$, defined as (Dansereau and Bruton 2007)

$$H_{ps}(\mathbf{s}) = \frac{R}{2R + L_s s_s + L_u s_u} \cdot \frac{R}{2R + L_t s_t + L_v s_v}, \tag{7}$$

and the corresponding 4-D IIR digital filter is obtained with the 2-D BLT as

$$T_{ps}(\mathbf{z}) = \frac{R}{2R + \sum_{k\in\{s,u\}} L_k \frac{z_k - 1}{z_k + 1}} \cdot \frac{R}{2R + \sum_{k\in\{t,v\}} L_k \frac{z_k - 1}{z_k + 1}}. \tag{8}$$

It is worthwhile to note that the frequency warping present in the BLT transforms the 4-D hyperplanar passbands to curvilinear shapes in the 4-D frequency domain given by the expression $\sum L_k \frac{e^{j\omega_k} - 1}{e^{j\omega_k} + 1} = 0$. With some algebraic manipulation, it can be shown that the curvilinear shape takes the form $\sum L_k \tan(\omega_k/2) = 0$.

The 4-D prototype networks of the 4-D non-separable filter and 2-D prototype networks of the 4-D partially-separable filters are realized as WDFs. Here, passive circuit components (of type resistor R and inductor L with Laplace impedance functions R and Ls_k, respectively, for each dimension $k = \{s, t, u, v\}$) are replaced by the corresponding WDF equivalent digital models (Rajapaksha et al. 2015). These models implement scattering behavior using first order difference equations along each of the dimensions. The scattering behavior is modeled using components connected as series and/or parallel branch impedances/admittances using

the WDF theory. The scattering is realized in the WDFs using memoryless linear combination circuits i.e., adapters.

It is worthwhile to note that the computational complexity of the proposed 4-D IIR filters is significantly lower compared to that of a 4-D FIR filter. The proposed 4-D non-separable IIR planar filter consists of first-order 4-D IIR hyperplanar filters and the proposed partially-separable 4-D IIR planar filter consists of first-order 2-D IIR hyperplanar filters. As pointed out in (Madanayake et al. 2013), the selectivity of a first-order 2-D IIR planar filter is approximately equal to that provides by an FIR filter of order 20×20. Therefore, the IIR filter saves more than 98% of arithmetic operations. Similar reduction in arithmetic operations can be achieved with the proposed 4-D IIR filters. Furthermore, even though the proposed IIR filter cannot be designed to have a linear-phase response, *zero-phase filtering* can be incorporated to achieve a linear-phase response as demonstrated in (Dansereau and Bruton 2003). The zero-phase filtering can be implemented by processing the output of a 2-D/4-D IIR hyperplanar filter with the same filter, however with flipping the input signal to filter (i.e., output of the first filter) with respect to all the dimensions. Even though the zero-phase filtering increases the computational complexity of an IIR filter by two times, the computational complexity is still significantly lower (more than 95%) compared to an equivalent FIR filter.

3.2.1 Wave digital realization of 4-D non-separable depth filter

The proposed WDF realization for the 4-D non-separable hyperplanar filter is shown in Fig. 4b. Note that the same WDF realization is employed for both 4-D non-separable hyperplanar filter. In this realization, one serial unconstrained adapter and three constrained series 3-port adapters are employed. Furthermore, zero initial conditions (ZICs) are indicated as ZIC blocks. The WDF design equations are used to calculate the constant multipliers (γ) in the WDF adapters. The design procedure involves calculation of a quantity known as "port resistance," which has the dimension of resistance, and then in turn, using port resistances to calculate the corresponding multiplier constants for the adapters. In accordance with the WDF principle (Fettweis 1986), the inductors are replaced by first order difference equation (one sample delay along its corresponding dimension followed by multiplication by -1) and capacitors are replaced by one sample delay along its corresponding dimension. For the WDF realization shown in Fig. 4b, the coefficients pertaining to each adapter are calculated as

$$R_0 = R_4 = R \tag{9a}$$
$$R_1 = R_0 + L_s \tag{9b}$$
$$R_2 = R_1 + L_t \tag{9c}$$
$$R_3 = R_4 + L_v. \tag{9d}$$

Furthermore, the coefficients γ_i of adaptors are calculated as

$$\gamma_1 = \frac{R_0}{R_1} \tag{10a}$$
$$\gamma_2 = \frac{R_1}{R_2} \tag{10b}$$
$$\gamma_3 = \frac{2R_2}{R_2 + L_u + R_3} \tag{10c}$$
$$\gamma_4 = \frac{2R_3}{R_2 + L_u + R_3} \tag{10d}$$

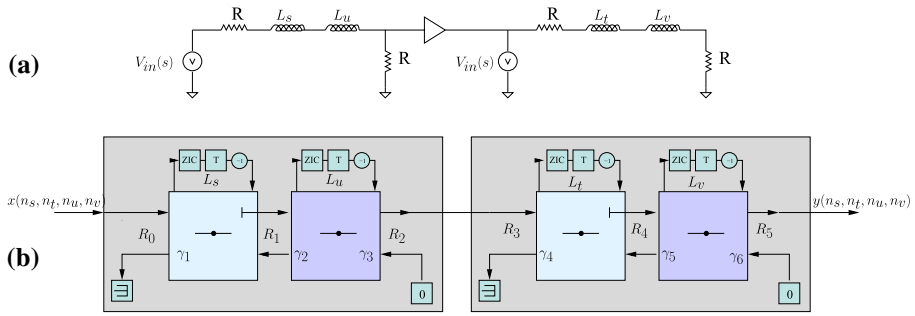

Fig. 5 **a** Passive prototype network employed for the 4-D partially-separable hyperplanar filter; **b** WDF realization

$$\gamma_5 = \frac{R_2}{R_3}. \tag{10e}$$

3.2.2 Wave digital realization of 4-D partially-separable depth filter

The proposed WDF realization for a 4-D partially-separable depth filter is shown in Fig. 5b. Here, two unconstrained series 3-port adapters are used along with two constrained series 3-port adapters. In this case, the adapter coefficients are obtained as

$$R_0 = R \tag{11a}$$
$$R_1 = R_0 + L_s \tag{11b}$$
$$R_3 = R_5 = R \tag{11c}$$
$$R_4 = R_3 + L_t. \tag{11d}$$

Furthemore, the coefficients γ_i of the adapters are calculated as

$$\gamma_1 = \frac{R_0}{R_1} \tag{12a}$$
$$\gamma_2 = \frac{2R_2}{R_2 + L_u + R_1} \tag{12b}$$
$$\gamma_3 = \frac{2R_1}{R_2 + L_u + R_1} \tag{12c}$$
$$\gamma_4 = \frac{R_3}{R_4} \tag{12d}$$
$$\gamma_5 = \frac{2R_4}{R_4 + L_v + R_5} \tag{12e}$$
$$\gamma_6 = \frac{2R_5}{R_4 + L_v + R_5}. \tag{12f}$$

3.3 Sensitivity to errors from coefficient quantization

In this subsection, we discuss the low-sensitivity proprieties of the WDFs. The 4-D transmission function for this doubly-terminated lossless 4-D network is (Bruton 1980) $t(\mathbf{s}, L_k) = \frac{2R}{2R+\sum L_k s_k}$ and 4-D reflectance function is $\rho(\mathbf{s}, L_k) = \frac{-\sum L_k s_k}{2R+\sum L_k s_k}$. The 4-D frequency

response of the transmission and reflectance functions are obtained by setting $s_k = j\omega_k$, where $\omega_k \in \mathbb{R}$. The inductance parameters L_k satisfy the 4-D Feldkeller equation (Bruton 1980)

$$\|t(j\boldsymbol{\omega}, L_k)\|^2 = 1 - \|\rho(j\boldsymbol{\omega}, L_k)\|^2 \tag{13}$$

The 4-D hyperplanar region defined by $\sum L_k\omega_k = 0$ denotes a 3-D manifold of resonance of the doubly-terminated passive network that defines the passband of the 4-D LF depth filter (Zhang and Bruton 1994; Dansereau and Bruton 2003). This resonant plane has $t(j\boldsymbol{\omega}, L_k) = 1$ and the region in $\boldsymbol{\omega}$ that lies close to the hyperplane of resonance satisfies $\|t(j\boldsymbol{\omega}, L_k)\|^2 \approx 1 - \|\rho(j\boldsymbol{\omega}, L_k)\|^2$. The gain sensitivity to inductance parameters takes the form

$$S_{L_k}^{\|t(j\boldsymbol{\omega}, L_k)\|} = -\frac{L_k}{\|t(j\boldsymbol{\omega}, L_k)\|}\left(\frac{\|\rho(j\boldsymbol{\omega}, L_k)\|}{\|t(j\boldsymbol{\omega}, L_k)\|}\right)\cdot\left(\frac{\partial\|\rho(j\boldsymbol{\omega}, L_k)\|}{\partial L_k}\right) \tag{14}$$

From the Feldkeller Equation, $\|\rho(j\boldsymbol{\omega}, L_k)\| = 0$ on the 4-D hyperplanar passband; also, $\|\rho(j\boldsymbol{\omega}, L_k)\|$ is a continuous non-negative function of L_k. Therefore, for a small ΔL_k, $L_k \pm \Delta L_k \geq 0$ leads to a corresponding change in the reflectance of $\Delta\|\rho(j\boldsymbol{\omega}, L_k)\| > 0$. Further, $\partial\|\rho(j\boldsymbol{\omega}, L_k)\|/\partial L_k = 0$, which implies that the gain sensitivity of the 4-D hyperplanar passband is zero valued, and is small valued on its neighborhood. Therefore, it is clear that the passband of the 4-D hyperplanar filter has very low sensitivity to deviations of the network synthesis parameters L_k. The degenerate cases for 2-D and 3-D doubly-terminated hyperplanar filters follow the same arguments for proving low-sensitivity.

4 Proposed raster-scanned FPGA architectures

Let the 4-D LF consist of a 4-D tensor, obtained from a uniformly spaced rectangular array of imaging cameras. Let there be N_s and N_t cameras along the s and t orthogonal dimensions, respectively, as shown in Fig. 6, where $(N_s, N_t, N_u, N_v) \in \mathbb{Z}^{4+}$. Each camera produces an image of resolution $N_u \times N_v$, leading to an LF of size $N_s \times N_t \times N_u \times N_v$. The proposed 4-D WDFs assume raster-scanned image samples, which scan through each image, first along rows, then along columns, starting with the top-left image and proceeding first along columns of images, until all rows are completed. Let the raster-scanned LF be denoted $w_{scan}(k)$ then, for $k \in \mathbb{N}$, the mapping between the 4-D tensor to raster-scan signal becomes $w_{scan}(k), k = n_s + n_t N_s + n_u N_s N_t + n_v N_s N_t N_u$. Here, $(n_s, n_t, n_u, n_v) \in \mathbb{Z}^4$ and $0 \leq n_s < N_s, 0 \leq n_t < N_t, 0 \leq n_u < N_u$, and $0 \leq n_v < N_v$, respectively. Because the filter is implemented as a raster-scanned (centralized) processor, the output of the filter will also be a 1-D raster-scanned output of the form $y_{scan}(k)$, which can subsequently indexed-mapped to obtain the either the entire 4-D LF output or one of the (typically the central) output sub aperture images as required by the application.

Unit delays along s, t, u, and v are unit increments of the integer variables n_s, n_t, n_u, and n_v, respectively, in the discrete domain, and corresponds to the 4-D z-domain unit delay operators $z_s^{-1}, z_t^{-1}, z_u^{-1}$, and z_v^{-1}, in the same order. The sampled 4-D LF can be considered as a 4-D z-domain input signal, denoted $W(\mathbf{z})$, which is filtered by the transmission function, given now in the z-domain as $T_{ns}(\mathbf{z})$ and $T_{ps}(\mathbf{z})$ [see (6) and (8), respectively] to produce the corresponding output LF $Y(\mathbf{z})$. We propose two WDF architectures operating on the raster scanned 4-D LF data: non-separable approach containing a cascade of two 4-D WDFs for $T_{ns}(\mathbf{z})$ (Fig. 7 shows one of the cascaded 4-D WDFs); partially-separable approach containing a cascade of two 2-D WDFs for $T_{ps}(\mathbf{z})$, as shown in Fig. 8. Both architectures shown in Fig. 7 and Fig. 8 present a graphical depiction of a structural hardware description

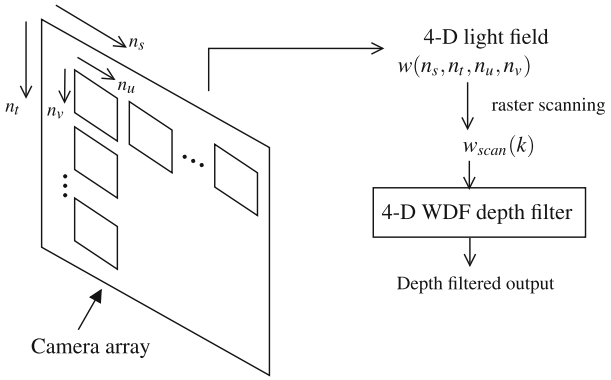

Fig. 6 Processing of a LF using the proposed 4-D WDFs

of the 4-D WDFs shown in Figs. 4b and 5b, respectively. The two architectures are based on 3-port series and parallel adapters (both unconstrained and reflection-free), and spatial delay processors (SDP) blocks realize ZICs at the edges of the 4-D computational grid for the s, t, and u bounded dimensions. The fourth dimension v is unbounded and does not require an SDP circuit as allowed by practical-BIBO stability criterion (Agathoklis and Bruton 1983). Both architectures use one unconstrained adapter, which is defined using two multiplier coefficients, and these adapters are located approximated in the central region of the architecture to ensure the critical path delay of the architecture becomes as low as possible. The WDF adapters are realized using basic blocks such as adders and multipliers available in Xilinx system generator tools and the SDP circuits are realized using FIFO buffers and multiplexers.

5 Experimental results

In this section, we present the experimental results obtained with the FPGA implementation of the proposed two 4-D WDF architectures. To this end, we first present the selection of word lengths of the FPGA implementations.

5.1 Selection of the fixed point word length

We employ a two-step method for the selection of the word lengths of the digital implementations. We first determine the word length of the adapter coefficients (W_{in}) by employing the mean-square error (MSE) between the impulse responses obtained with the FPGA implementation and the software implementation with MATLAB as a quantitative metric. Then, the data path (i.e., the word length of the systems, W_{sys}) is determined as the word length that results no overflow or saturation with the selected W_{in}. The MSEs obtained for both 4-D non-separable and partially-separable IIR filters with different lengths for the fractional parts (D_{in} and D_{sys}) are shown in Fig. 9. We select W_{in} and W_{sys} as 13 bits and 15 bits, respectively, for both WDF implementations. Furthermore, for both W_{in} and W_{sys}, the integer part contains 2 bits, and the fractional part contains 11 bits for adapter coefficients D_{in} and 13 bits for the data path D_{sys}. The considered inputs were quantized to 8-bits.

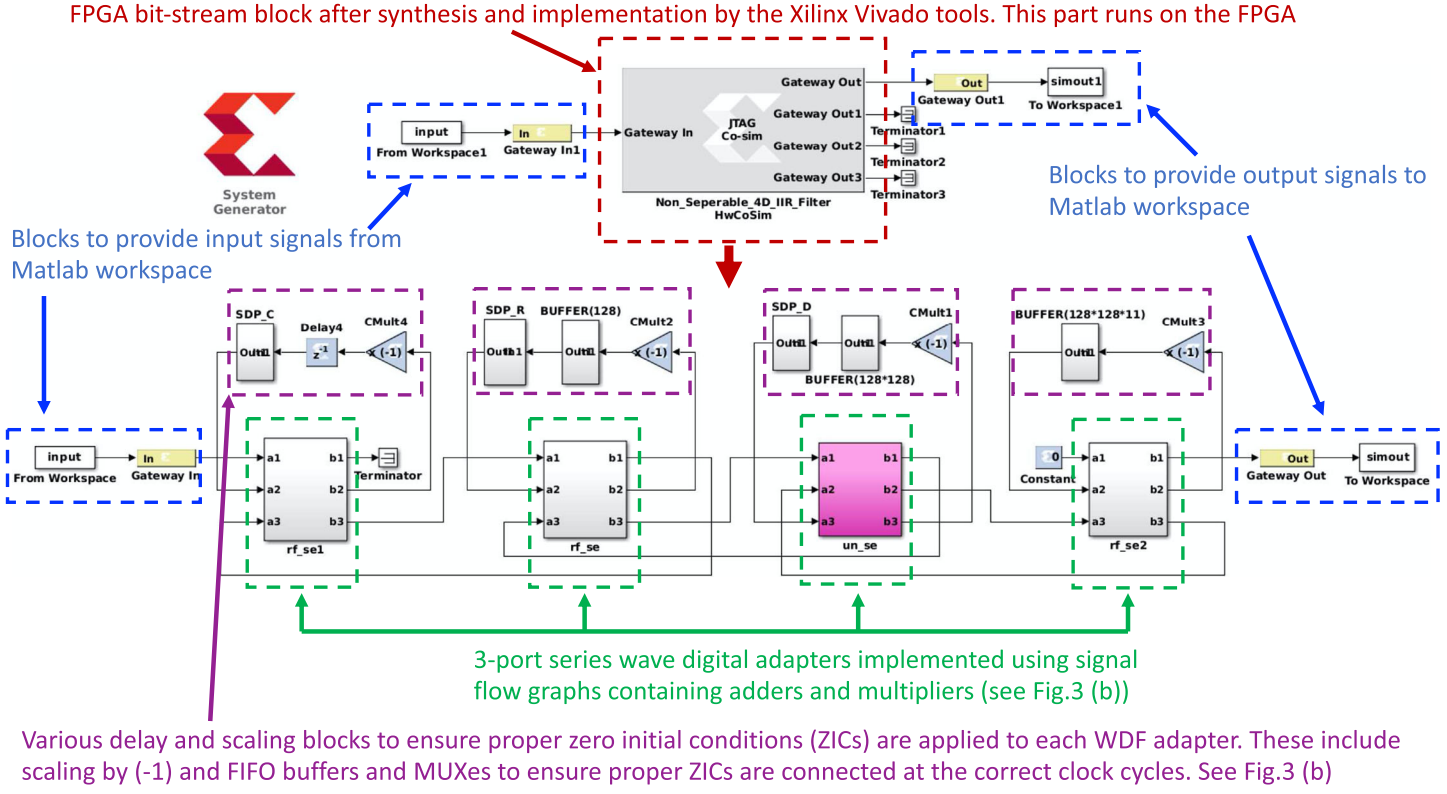

Fig. 7 FPGA architecture of a 4-D non-separable WDF. The WDF adapter architecture shown in Fig. 4b is implemented using Xilinx Vivado system generator tools, which allows a structural implementation of the proposed WDF using FPGA specific Simulink blocks such as adders, multipliers, delays, buffers and multiplexers. The graphical form of the FPGA design shown here has a one-to-one correspondence with the WDF block diagram architecture shown in Fig. 4b, where each WDF adapter is now realised using FPGA specific Simulink blocks and the ZICs are provided by means of special circuits (enclosed with purple dotted lines) consisting of FIFO buffers, scaling blocks and multiplexers, that ensure zero valued inputs are connected to each WDF adapter at the correct clock edges

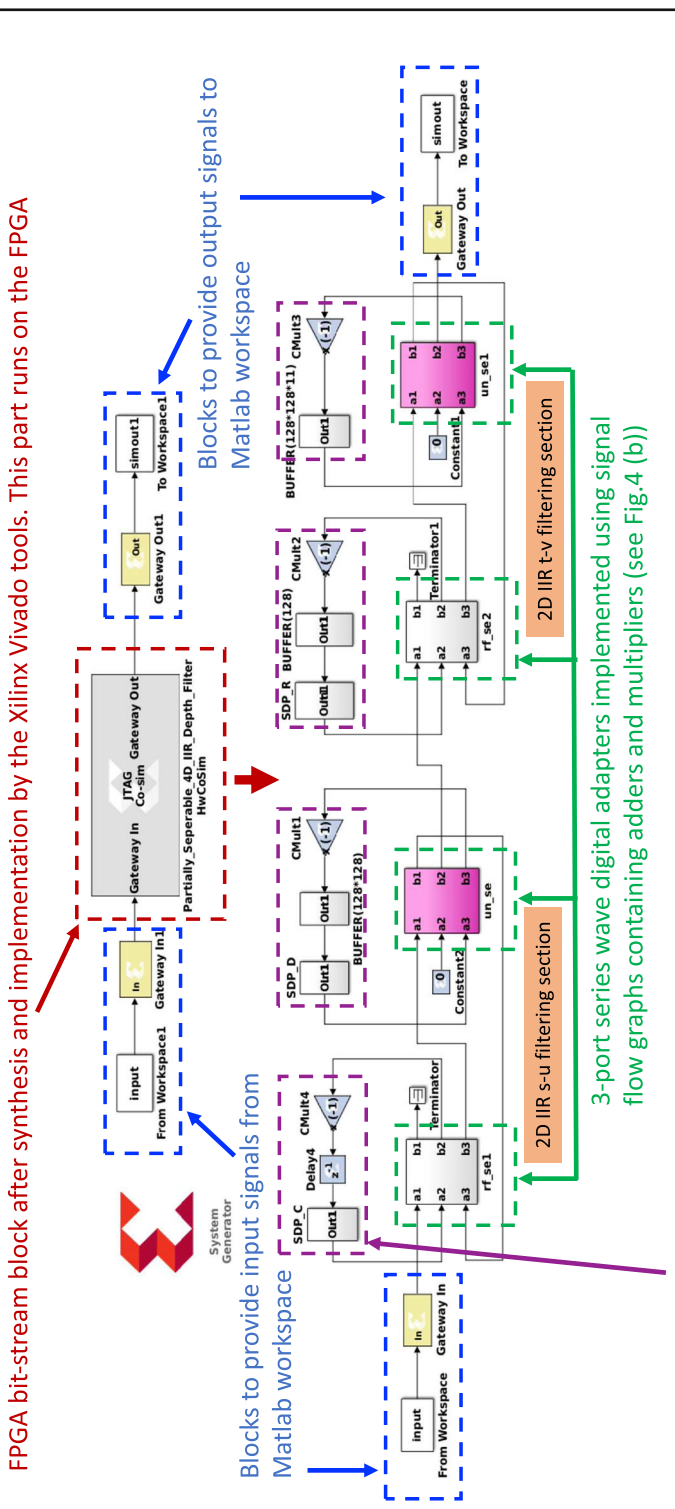

Fig. 8 FPGA architecture of a 4-D partially-separable WDF. The WDF adapter architecture shown in Fig. 5b is implemented using Xilinx Vivado system generator tools, which allows a structural implementation of the proposed WDF using FPGA specific Simulink blocks such as adders, multipliers, delays, buffers and multiplexers. The graphical form of the FPGA design shown here has a one-to-one correspondence with the WDF block diagram architecture shown in Fig. 5b, where each WDF adapter is now realised using FPGA specific Simulink blocks and the ZICs are provided by means of special circuits (enclosed with purple dotted lines) consisting of FIFO buffers, scaling blocks and multiplexers, that ensure zero valued inputs are connected to each WDF adapter at the correct clock edges

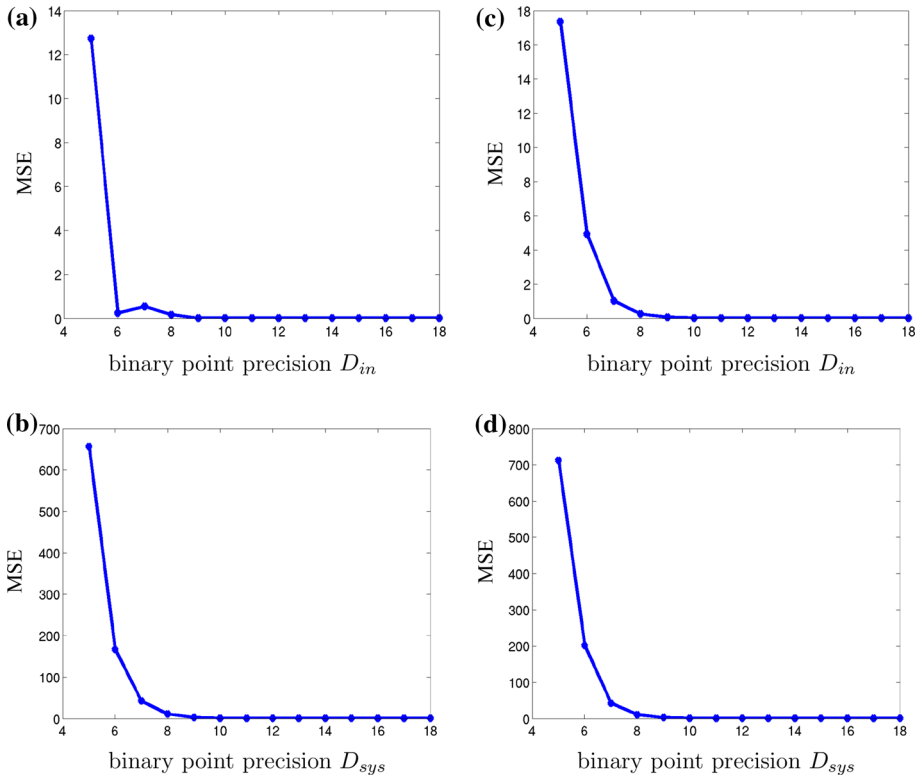

Fig. 9 MSE for the fractional-part word length of the adapter coefficients D_{in} **a** 4-D non-separable IIR filter, **c** 4-D partially-separable IIR filter; MSE for the fractional-part word length of the system D_{sys}, **b** 4-D non-separable IIR filter, **d** 4-D partially-separable IIR filter

5.2 Hardware co-simulation of the FPGA implementations

Both architectures are implemented on a Xilinx Virtex 6 Sx35 FPGA available with an ML605 prototyping board using MATLAB/Simulink and Xilinx system generator. The frequency responses of both architectures are verified using the unit impulse responses obtained with the FPGA implementations of the 4-D non-separable and partially-separable WDFs. Furthermore, real-time operation of both architectures are verified using bit-true and cycle-accurate hardware co-simulations.

We consider a typical example of post-capture refocusing of a LF of size $11 \times 11 \times 128 \times 128$ with the proposed 4-D WDFs. To this end, the 4-D non-separable WDF is designed with $\gamma_1 = 0.5556$, $\gamma_2 = 0.72$, $\gamma_3 = 1.087$, $\gamma_4 = 0.652$ and $\gamma_5 = 0.75$ and a 4-D partially-separable WDF is designed with $\gamma_1 = \gamma_4 = 0.5556$, $\gamma_2 = \gamma_5 = 1.0588$ and $\gamma_3 = \gamma_6 = 0.5882$. The resource consumption of the FPGA for the two WDF implementations are presented in Table 1. Available resources of the FPGA are sufficient for the implementation of the 4-D partially-separable WDF. However, only one 4-D hyperplanar filter out of the two hyperplanar filters is implemented for the 4-D non-separable WDF. Note that, this does not affect to the verification of the FPGA architecture of the 4-D non-separable WDF because both 4-D hyperplanar filters have similar transfer functions with the same coefficients. Similar to the reduction of the processing time achieved with the software implementation of a 4-D

Table 1 Design parameters and FPGA metrics for the WDF implementations of a 4-D non-separable WDF (single hyperplanar filter) and a 4-D partially-separable WDF (both hyperplanar filters)

Design parameter/FPGA metric	Non-separable WDF	Partially-separable WDF
W_{in}, D_{in}	13, 11	13, 11
W_{sys}, D_{sys}	15, 12	15, 12
N_s	11	11
N_t	11	11
N_u	128	128
N_v	128	128
Clock frequency (MHz)	33.35	33.37
Number of occupied slices	1065	1350
Number of slice registers	884	900
Number of slice LUTs	478	3006
Number of LUT flip-flop pairs	2587	3127
Number of IOBs	2	2
Number of RAMB36E1s	386	386

partially-separable hyperplanar filter compared to that of a 4-D non-separable hyperplanar filter (Dansereau and Bruton 2007), the FPGA implementation of the 4-D partially-separable WDF saves approximately 40% of resources compared to the 4-D non-separable WDF, except IOBs and RAMB36E1s. For LFs of size $N_s \times N_t \times N_u \times N_v$, the real-time throughput is $F_{clock}/N_s N_t N_u N_v$, where F_{clock} is the real-time clock of the FPGA. Both architectures achieve a throughput of 16.8 LFs/s for a gray-scale LF. For a color LF comprising of red, green, and blue components, a throughput of 5.6 LFs/s is achieved because each color component can be processed as a gray-scale LF.

The unit-impulse responses of the two WDF implementations are obtained with bit-true and cycle-accurate hardware co-simulation, and the 4-D frequency responses are obtained by computing the 4-D discrete-space Fourier transform of the unit-impulse responses. Figure 10 shows a few 2-D slices of the 4-D frequency responses obtained with the MATLAB simulation and the FPGA implementation for the 4-D non-separable hyperplanar WDF whereas Fig. 11 shows the same for the 4-D partially-separable WDF. The signal to noise ratios computed using the unit-impulse responses obtained with the MATLAB simulations and FPGA implementations (i.e. $10 \log_{10} \frac{\sum_{4-\mathbf{D}} h_{MATLAB}(\mathbf{n})^2}{\sum_{4-\mathbf{D}} h_{Error}(\mathbf{n})^2}$) are 61.231 dB and 59.718 dB for the proposed 4-D non-separable and partially-separable WDF architectures, respectively. These signal to noise ratio values verify the correct operation of the both FPGA implementations.

A cropped LF of size $11 \times 11 \times 128 \times 128$ obtained from the LF "Swans_1" (original size $= 15 \times 15 \times 434 \times 625$) in the EPFL LF dataset (Rerabek and Ebrahimi 2016) is processed with MATLAB implementations and the proposed FPGA implementations of the 4-D non-separable hyperplanar WDF and the 4-D partially separable WDF. Sub-aperture images of the input, outputs and the error between two out puts are shown in Fig. 12. The maximum errors between the outputs of the MATLAB implementations and the FPGA implementations are found to be 2.35% for both the proposed WDF architectures, which confirms the real-time correct operation of the proposed WDF architectures.

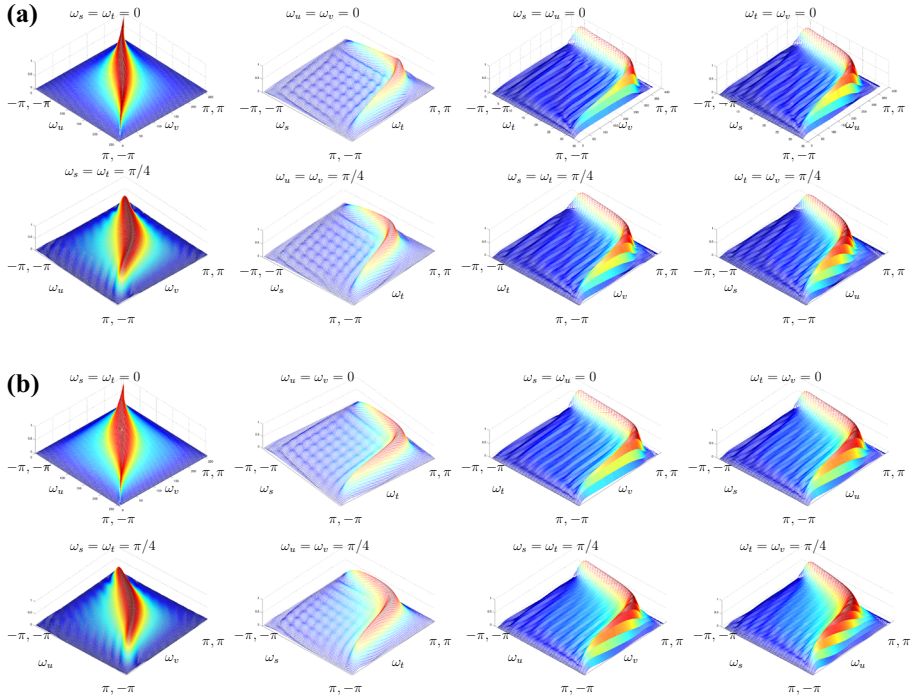

Fig. 10 Selected 2-D slices of the frequency response of the 4-D non-separable hyperplanar WDF $|T_{ns}^{s,u}(e^{j\omega_s}, e^{j\omega_t}, e^{j\omega_u}, e^{j\omega_v})|$ for $\omega_s = \omega_t = 0, \omega_u = \omega_v = 0, \omega_s = \omega_u = 0, \omega_t = \omega_v = 0, \omega_s = \omega_t = \frac{\pi}{4}$, $\omega_u = \omega_v = \frac{\pi}{4}, \omega_s = \omega_u = \frac{\pi}{4}$ and $\omega_t = \omega_v = \frac{\pi}{4}$ **a** MATLAB simulation, **b** FPGA implementation

5.3 Comparison with previously-reported FPGA architectures

To the best of our knowledge, the proposed design is the first reported 4-D WDF architecture with prototype FPGA implementation. Previously-reported FPGA architectures for 4-D depth filtering in LFs are based on direct-, differential-, and integral-form signal flow graphs with different level of parallelism along the s, t, u, and v dimensions. Table 2 provides a comparison with these architectures. It should be noted that the operational speed of these designs depend on the FPGA family and the proposed 4-D WDF is currently implemented on a Xilinx Virtex-6 series device, which implies lower speed range than more recent Virtex-7 series of Xilinx FPGA devices. Because the proposed filters are synthesized based on MD passive prototype networks having low-sensitivity properties (Temes and Orchard 1973; Bruton 1980) and WDF realizations inherently provide the lowest sensitivity to perturbation of filter parameters (Fettweis 1986) while retaining the structure of the underlying MD passive prototype network, the proposed 4-D WDF architecture leads to a robust implementation in terms of coefficient quantization effects and filter parameter perturbations.

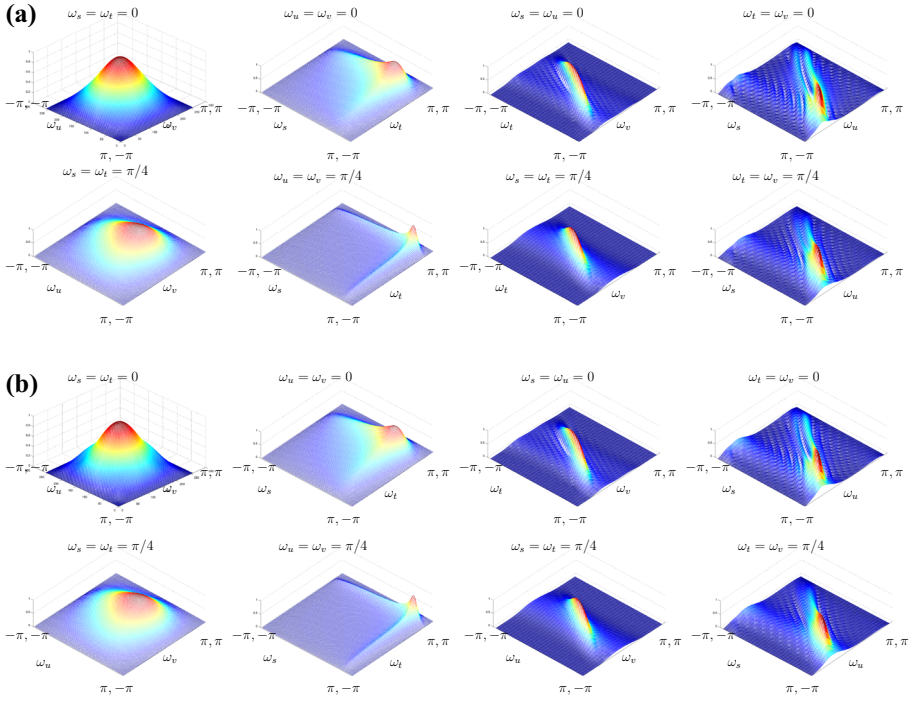

Fig. 11 2D slices of the frequency response of the 4-D partially-separable WDF $|T_{ps}(e^{j\omega_s}, e^{j\omega_t}, e^{j\omega_u}, e^{j\omega_v})|$ for $\omega_s = \omega_t = 0$, $\omega_u = \omega_v = 0$, $\omega_s = \omega_u = 0$, $\omega_t = \omega_v = 0$, $\omega_s = \omega_t = \frac{\pi}{4}$, $\omega_u = \omega_v = \frac{\pi}{4}$, $\omega_s = \omega_u = \frac{\pi}{4}$ and $\omega_t = \omega_v = \frac{\pi}{4}$ **a** MATLAB simulation, **b** FPGA implementation

6 Conclusions and future work

WDF realizations of 4-D non-separable and partially-separable IIR hyperplanar filters are proposed in this paper for depth-based enhancement of LFs. The closed-form equations are derived to compute the WDF coefficients of both realizations. This enables fast tuning of the passband for a given depth of a scene captured in an LF. To the best of our knowledge, the proposed 4-D WDFs are the first filters employed for depth-based enhancement of LFs. Raster-scanned FPGA architectures are proposed for both 4-D WDF filters and implemented on a Xilinx Virtex 6 Sx35 FPGA. The unit-impulse responses obtained with the bit-true and cycle-accurate hardware co-simulation of the FPGA implementations of both architectures well agree with those obtained using the software implementations using MATLAB. Furthermore, experimental results obtained for refocusing of the LF "Swans_1" confirm the real-time operation of the proposed WDF filters. In particular, a real-time throughout of 16.8 LFs/s for a gray-scale LF of size $11 \times 11 \times 128 \times 128$ can be achieved with the FPGA implementation of 4-D partially-separable WDF. The proposed WDF architectures lead to robust implementation in terms of coefficient quantization effects and filter parameter perturbations due to the inherent low-sensitivity properties WDF realizations. Future work includes to extension of the WDF architectures to enhancement of 5-D light field videos based on both depth and velocity using 5-D IIR hyperplanar filters.

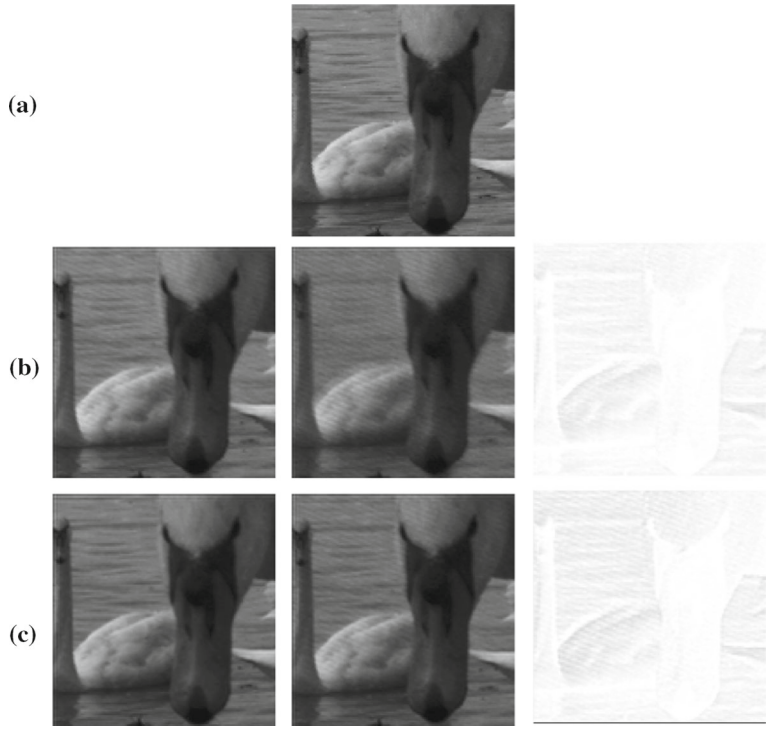

Fig. 12 **a** A sub-aperture image of the cropped input LF "Swans_1" of size $11 \times 11 \times 128 \times 128$; **b** a sub-aperture image of the output obtained with the 4-D non-separable hyperplanar WDF (left) from MATLAB implementation (center) FPGA implementation (right) the error between the two outputs; **c** a sub-aperture image of the output obtained with the 4-D partially-separable WDF (left) from MATLAB implementation (center) FPGA implementation (right) the error between the two outputs; the color is inverted for better viewing, i.e., white = 0% and black = 100%

Table 2 Comparison with previously-reported FPGA architectures

Design	Filter type and architecture	Level of parallelism	Implementation platform	Performance
(Liyanage et al. (2019))	4-D IIR, multi-passband, depth-filtering, direct-form realization	Systolic array (fully parallel) along s, t and partially parallel along u/v	Xilinx Virtex-7 FPGA	135 MHz max clock speed (critical path delay of 7.4 ns)
(Hahne and Aggoun (2014b))	FIR filter based shift-sum refocusing	Partially (2-D) parallel	Xilinx Spartan-6 FPGA	Overall throughput 60 frames/s, critical path delay is not reported
(Madanayake et al. (2011b))	4-D IIR, single-passband, depth-filter, direct-form realization	Fully-centralized (raster scanned along s, t, u, v)	Xilinx Virtex-4 FPGA	18 MHz max frequency
(Wimalagunarathne et al. (2012))	4-D IIR, single-passband, depth-filter, direct-form realization	Systolic array along s, t and raster-scanned along u, v	Xilinx Virtex-6 FPGA	39 MHz max frequency

Table 2 continued

Design	Filter type and architecture	Level of parallelism	Implementation platform	Performance
(Madanayake et al. (2015))	4-D IIR, depth-filter, non-separable, differential-form realization	Fully-centralized (raster scanned along s, t, u, v)	Xilinx Virtex-6 FPGA	55 MHz max frequency
(Wimalagunarathne et al. (2013))	4-D IIR, depth-filter, non-separable, Integral-form realization	Fully-centralized (raster scanned along s, t, u, v)	Xilinx Virtex-6 FPGA	35 MHz max frequency
Proposed	4-D IIR, depth-filter, partially separable and non-separable versions, 4-D WDF realization	Fully-centralized (raster scanned along s, t, u, v)	Xilinx Virtex-6 FPGA	33 MHz max frequency

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